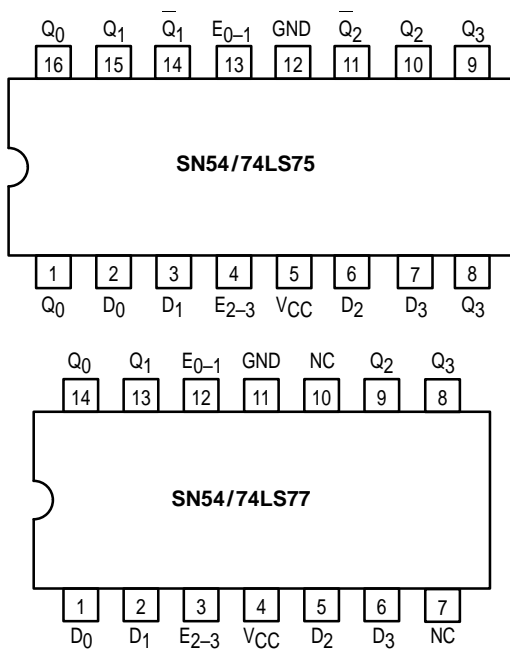# MOTOROLA

# 4-BIT D LATCH

The TTL/MSI SN54/74LS75 and SN54/74LS77 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The SN54/74LS75 features complementary Q and Q output from a 4-bit latch and is available in the 16-pin packages. For higher component density applications the SN54/74LS77 4-bit latch is available in the 14-pin package with Q outputs omitted.

## CONNECTION DIAGRAMS DIP (TOP VIEW)

| Pin | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |
|---|---|---|---|---|---|---|---|---|
| Top | $Q_0$ | $Q_1$ | $\overline{Q_1}$ | $E_{0-1}$ | GND | $\overline{Q_2}$ | $Q_2$ | $Q_3$ |

**SN54/74LS75**

| Pin | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| Bottom | $Q_0$ | $D_0$ | $D_1$ | $E_{2-3}$ | $V_{CC}$ | $D_2$ | $D_3$ | $Q_3$ |

| Pin | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| Top | $Q_0$ | $Q_1$ | $E_{0-1}$ | GND | NC | $Q_2$ | $Q_3$ |

**SN54/74LS77**

| Pin | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| Bottom | $D_0$ | $D_1$ | $E_{2-3}$ | $V_{CC}$ | $D_2$ | $D_3$ | NC |

## PIN NAMES

| | | LOADING (Note a) | |
|---|---|---|---|
| | | HIGH | LOW |
| $D_1$–$D_4$ | Data Inputs | 0.5 U.L. | 0.25 U.L. |
| $E_{0-1}$ | Enable Input Latches 0, 1 | 2.0 U.L. | 1.0 U.L. |
| $E_{2-3}$ | Enable Input Latches 2, 3 | 2.0 U.L. | 1.0 U.L. |
| $\overline{Q_1}$–$\overline{Q_4}$ | Latch Outputs (Note b) | 10 U.L. | 5 (2.5) U.L. |
| $Q_1$–$Q_4$ | Complimentary Latch Outputs (Note b) | 10 U.L. | 5 (2.5) U.L. |

NOTES:
a) 1 Unit Load (U.L.) = 40 µA HIGH.
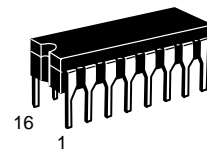b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

## TRUTH TABLE
### (Each latch)

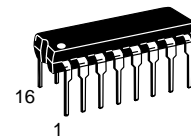| $t_n$ | $t_{n+1}$ |
|---|---|
| D | Q |
| H | H |
| L | L |

NOTES:
$t_n$ = bit time before enable negative-going transition
$t_{n+1}$ = bit time after enable negative-going transition
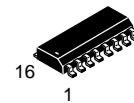
---

# SN54/74LS75
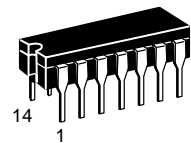# SN54/74LS77

## 4-BIT D LATCH
### LOW POWER SCHOTTKY
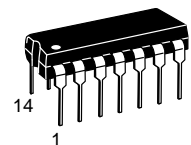
**J SUFFIX**
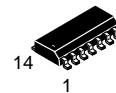CERAMIC
CASE 620-09
16
1

**N SUFFIX**
PLASTIC
CASE 648-08
16
1

**D SUFFIX**
SOIC
CASE 751B-03
16
1

**J SUFFIX**
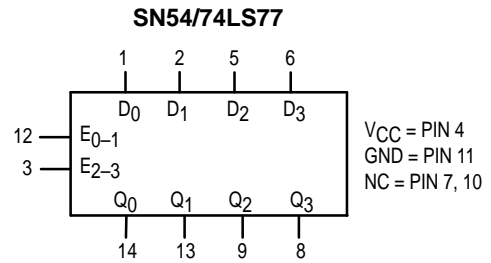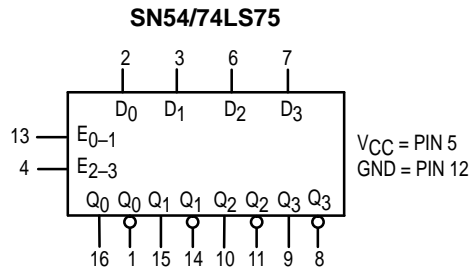CERAMIC
CASE 632-08
14
1

**N SUFFIX**
PLASTIC
CASE 646-06
14
1

**D SUFFIX**
SOIC
CASE 751A-02
14
1

## ORDERING INFORMATION

| | |
|---|---|
| SN54LSXXJ | Ceramic |
| SN74LSXXN | Plastic |
| SN74LSXXD | SOIC |

---

FAST AND LS TTL DATA

# SN54/74LS75

## LOGIC SYMBOLS

**SN54/74LS75**

```
        2    3    6    7
        D0   D1   D2   D3
   13 — E0–1
    4 — E2–3                    VCC = PIN 5
        Q0 Q0 Q1 Q1 Q2 Q2 Q3 Q3   GND = PIN 12
        16  1 15 14 10 11  9  8
```

**SN54/74LS77**

```
        1    2    5    6
        D0   D1   D2   D3
   12 — E0–1                    VCC = PIN 4
    3 — E2–3                    GND = PIN 11
        Q0    Q1    Q2    Q3    NC = PIN 7, 10
        14    13     9     8
```

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| Symbol | Parameter | | Limits | | | Unit | Test Conditions | |
|--------|-----------|---|-----|-----|-----|------|-----------------|---|
| | | | Min | Typ | Max | | | |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | | 0.8 | | | |
| $V_{IK}$ | Input Clamp Diode Voltage | | | −0.65 | −1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = −18 mA | |
| $V_{OH}$ | Output HIGH Voltage | 54 | 2.5 | 3.5 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | |
| | | 74 | 2.7 | 3.5 | | V | | |
| $V_{OL}$ | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | $I_{OL}$ = 4.0 mA | $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | $I_{OL}$ = 8.0 mA | |
| $I_{IH}$ | Input HIGH Current | D Input E Input | | | 20 80 | μA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V | |
| | | D Input E Input | | | 0.1 0.4 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V | |
| $I_{IL}$ | Input LOW Current | D Input E Input | | | −0.4 −1.6 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V | |
| $I_{OS}$ | Short Circuit Current (Note 1) | | −20 | | −100 | mA | $V_{CC}$ = MAX | |
| $I_{CC}$ | Power Supply Current | | | | 12 | mA | $V_{CC}$ = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

**AC CHARACTERISTICS** ($T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Symbol | Parameter | | Limits | | Unit | Test Conditions |
|--------|-----------|-----|-----|-----|------|-----------------|
| | | Min | Typ | Max | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay, Data to Q | | 15 9.0 | 27 17 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay, Data to $\overline{Q}$ | | 12 7.0 | 20 15 | ns | $V_{CC}$ = 5.0 V $C_L$ = 15 pF |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay, Enable to Q | | 15 14 | 27 25 | ns | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay, Enable to $\overline{Q}$ | | 16 7.0 | 30 15 | ns | |

# SN54/74LS77

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

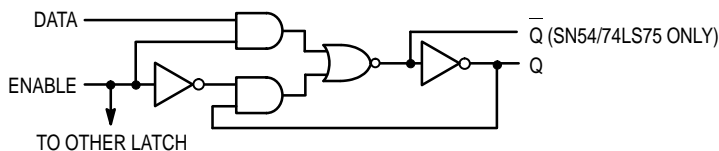| Symbol | Parameter | | Min | Typ | Max | Unit | Test Conditions | |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs | |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs | |
| | | 74 | | | 0.8 | | | |
| $V_{IK}$ | Input Clamp Diode Voltage | | | −0.65 | −1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = −18 mA | |
| $V_{OH}$ | Output HIGH Voltage | 54 | 2.5 | 3.5 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | |
| | | 74 | 2.7 | 3.5 | | V | | |
| $V_{OL}$ | Output LOW Voltage | 54, 74 | | 0.25 | 0.4 | V | $I_{OL}$ = 4.0 mA | $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | $I_{OL}$ = 8.0 mA | |
| $I_{IH}$ | Input HIGH Current | D Input E Input | | | 20 80 | μA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V | |
| | | D Input E Input | | | 0.1 0.4 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V | |
| $I_{IL}$ | Input LOW Current | D Input E Input | | | −0.4 −1.6 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V | |
| $I_{OS}$ | Short Circuit Current (Note 1) | | −20 | | −100 | mA | $V_{CC}$ = MAX | |
| $I_{CC}$ | Power Supply Current | | | | 13 | mA | $V_{CC}$ = MAX | |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

**AC CHARACTERISTICS** ($T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay, Data to Q | | 11 9.0 | 19 17 | ns | $V_{CC}$ = 5.0 V $C_L$ = 15 pF |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay, Enable to Q | | 10 10 | 18 18 | ns | |

# SN54/74LS75 ● SN54/74LS77

**LOGIC DIAGRAM**

DATA

ENABLE

$\overline{Q}$ (SN54/74LS75 ONLY)

Q

TO OTHER LATCH

## GUARANTEED OPERATING RANGES

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V |
| $T_A$ | Operating Ambient Temperature Range | 54<br>74 | −55<br>0 | 25<br>25 | 125<br>70 | °C |
| $I_{OH}$ | Output Current — High | 54, 74 | | | −0.4 | mA |
| $I_{OL}$ | Output Current — Low | 54<br>74 | | | 4.0<br>8.0 | mA |

## AC SETUP REQUIREMENTS ($T_A$ = 25°C, $V_{CC}$ = 5.0 V)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $t_W$ | Enable Pulse Width High | 20 | | | ns | |
| $t_S$ | Setup Time | 20 | | | ns | $V_{CC}$ = 5.0 V |
| $t_h$ | Hold Time | 0 | | | ns | |

**AC WAVEFORMS**

D

1.3 V          1.3 V

$t_s$          $t_h$

E

1.3 V    1.3 V          1.3 V

$t_{PLH}$

Q

$t_{PLH}$    1.3 V          $t_{PHL}$    1.3 V

$t_{PHL}$

Q

$t_{PHL}$    1.3 V          $t_{PLH}$    1.3 V

$t_{PHL}$          $t_{PLH}$
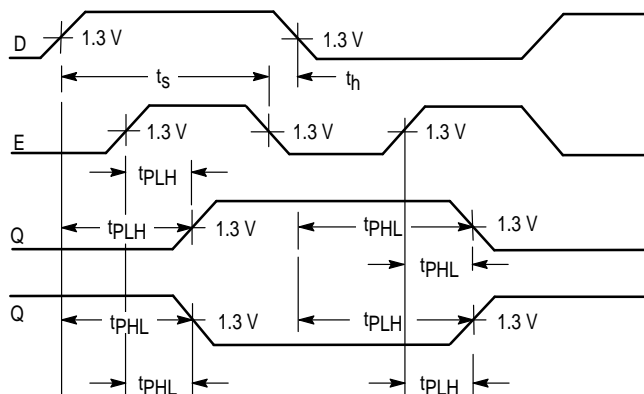
## DEFINITION OF TERMS

SETUP TIME ($t_S$) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME ($t_h$) — is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.